IN THE CLAIMS

Cancel claims 1-21 without prejudice or disclaimer, and add new claims 22-27 as follows:

22. (New) A data processing device comprising:

a first processing unit having an integer calculation function;

a second processing unit whose controlled by the first processing unit having a fixed-point data calculation function;

wherein the second processing unit includes a multiplier which is performance an integer data calculation and a fixed-point data calculation;

wherein the first processing unit performs a first type instruction, and the second processing unit performs a second type instruction, the second type instruction having a first instruction for calculating an integer data and a second instruction for calculating a fixed-point data;

wherein the first processing unit decodes the first type instruction and the second type instruction,

wherein the first processing unit outputs a control signal corresponding to a decoded result to the second processing unit when the first processing unit decodes the second instruction,

wherein when the first processing unit decodes the first type instruction, the first processing unit operates,

wherein when the first processing unit decodes the first instruction of the second type instruction, the multiplier in the second processing unit calculates an integer data,

wherein when the first processing unit decodes the second instruction of the second type instruction, the multiplier in the second processing unit calculates a fix-point data.

wherein when a second instruction is executed to transfer data, whose bit length is shorter than the bit length of the register, from the register to the outside of the second processing unit, the second processing unit outputs a required bit length of the data from the higher-order side of the register to the outside.

23. (New) A data processing device according to claim 22,

wherein the multiplier has a shifter,

wherein when the first processing unit decodes the first instruction of the second type instruction, the shifter outputs the output of the multiplier without shifting it,

wherein when the first processing unit decodes the second instruction of the second type instruction, the shifter outputs the output of the multiplier with shifting it.

24. (New) A data processing device according to claim 23,

wherein the first processing unit decodes the second instruction of the second type instruction, the shifter shifts left the output of the multiplier by one bit and inputs zero to the least significant bit.

25. (New) A data processing device according to claim 22,

wherein the first and second processing units are formed on a single semiconductor substrate.

26. (New) A data processing device according to claim 22, further comprising:

a first memory;

a second memory;

a first data bus coupled with the first processing unit, the second processing unit, the first memory and the second memory;

a second data bus coupled with the second processing unit and the first memory; and

a third data bus coupled with the second processing unit and the second memory.

27. (New) A data processing device according to claim 22, further comprising:

a first memory; and

a second memory,

wherein the second processing unit reds data from the first memory and the second memory in parallel.